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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,641	05/19/2004	Der-Yuan Tseng	12915-US-PA	3640

31561 7590 02/09/2007

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
SIM, YONG H	
ART UNIT	PAPER NUMBER
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/709,641	TSENG ET AL.	
	Examiner	Art Unit	
	Yong Sim	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-24* is/are allowed.

6)☒ Claim(s) *1 and 4-10* is/are rejected.

7)☒ Claim(s) *2, 3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *4/26/2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Taiwan, R. O. C. on 03/18/2004

Drawings

1. The drawings are objected to under 37 CFR 1.83(a) because they fail to show 302, 304, 306, 308, Cgs, Cgd, 402, 404, 406 and 408 as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and

informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. Figure 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furuhashi et al. (US 5,731,796, herein after "Furuhashi") in view of Yamamoto et al. (US 6,844,769 B2, herein after "Yammamoto").

Re claim 1, Furuhashi teaches a source driver ("Signal Drive Circuit" 1801, Fig. 18) for driving sources of a plurality of thin film transistors ("TFT" 502, Fig. 5), the source driver comprising: a shift register ("Shift Register" 2505, Fig. 25), for receiving digital image data; a latch ("Latch Circuit" 2507, Fig. 25), coupled to the shift register, for receiving digital image data from the shift register; a level shifter ("Level Shifter" 2511, Fig. 25), coupled to the latch, for receiving digital image data from the latch and for shifting a voltage level of digital image data; and an analog circuit ("D/A converter" 2513, Fig. 25. D/A converter circuit outputs an analog signal, therefore the circuit is an analog circuit.), coupled to the level shifter, for receiving the digital image data, converting the digital image data to a corresponding analog image data, and outputting the analog image data to the plurality of sources (Col. 2, lines 4 – 15; "Reference 2401 and 2402 represent signal drive circuits for acquiring the digital data transferred via signal drive circuit and converting the data into LCD voltages corresponding to the data to cause scanning lines to activate.");

But does not teach a power supply voltage level and a ground voltage level that are provided to the level shifter and the analog circuit; at least one middle voltage level

between the power supply voltage level and the ground voltage level is provided to the level shifter and the analog circuit.

However, Yamamoto teaches a drive circuit comprising a level shift circuit and amplitude expansion circuit wherein VDD (power supply potential), VH (second power supply potential), VM (intermediate power supply potential) and ground are supplied to drive the circuit (Col. 5, lines 35 – 46).

Therefore, taking the combined teachings of Furuhashi and Yammamoto, as a whole, it would have been obvious to a person having ordinary skill in the art to incorporate the level shift circuit as taught by Yammamoto to the source driver of Furuhashi to obtain a source driver with a level shift circuit which could output a breakdown voltage required for a power switching circuit of a drive-stage circuit using only low-voltage elements (Col. 2, lines 43 – 50).

Re claim 4, the combined teachings of Furuhashi and Yammamoto teach the source driver of claim 1, wherein the latch further comprises a first level latch ("Latch Circuit" 2507, Fig. 25) and a second level latch ("Latch Circuit" 2509, Fig. 25), wherein the first level latch sequentially receives digital image data, and digital image data comprises image data of horizontal lines, and the horizontal lines are sequentially arranged, when the first latch completely receives image data of one horizontal line, the first latch outputs image data of the one horizontal line to the second level latch, and continues receiving image data of next horizontal line, the second level latch outputs the image data of the one horizontal line to the level shifter (Col. 5, lines 24 – 35; "After the

display data for 1 horizontal line have been acquire by the latch circuit 2507, the data are transferred and stored in the latch circuit 2508." Col. 6, lines 20 – 25; "The data stored in the latch circuit 2509 is processed via the data bus 2510 in the level shifter for the voltage conversion.")

6. Claims 5 – 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furuhashi in view of Yammamoto, and further in view of Wang et al. (US 6,552,708 B1, hereinafter known as Wang).

Re claim 5, the combined teachings of Furuhashi and Yammamoto teach the source driver of claim 1, wherein the analog circuit with the positive polarity comprises a digital-to-analog converter ("D/A converter" 2513, Fig. 25) with the positive polarity (Col. 6, lines 8 – 12; "the digital-to-analog converting circuit can be constructed as to produce the lcd apply voltages having the positive polarity and the negative polarity.").

But does not disclose an output buffer.

However, Wang discloses an output buffer connected to DAC (Fig. 1, Col. 1 lines 35 – 37; "OP amp in the negative feedback connection to be a unit gain buffer.").

Therefore, taking the combined teachings of Furuhashi, Yammamoto and Wang, as a whole, it would have been obvious to a person having ordinary skill in the art to incorporate the output buffer taught by Wang to the source driver of Furuhashi and Yammamoto to obtain a source driver with a buffer connected to DAC to perform the data line driving for every state of the driver (Col. 1, lines 23 – 32).

Re claim 6, the combined teachings of Furuhashi, Yammamoto and Wang as a whole teach the source driver of claim 5, wherein the digital-to-analog converter with the positive polarity provides an image data conversion with the positive polarity (Col. 6, lines 8 – 12; "the digital-to-analog converting circuit can be constructed as to produce the lcd apply voltages having the positive polarity and the negative polarity.").

The limitations of claim 7 are substantially similar to the limitations of claim 5. Therefore it has been analyzed and rejected similar to the rejection of claim 5.

Re claim 8, the combined teachings of Furuhashi and Yammamoto teach the source driver of claim 1, wherein the analog circuit with the negative polarity comprises a digital-to-analog converter ("D/A converter" 2513, Fig. 25) with the positive polarity (Col. 6, lines 8 – 12; "the digital-to-analog converting circuit can be constructed as to produce the lcd apply voltages having the positive polarity and the negative polarity.").

But does not disclose an output buffer.

However, Wang discloses an output buffer connected to DAC (Fig. 1, Col. 1 lines 35 – 37; "OP amp in the negative feedback connection to be a unit gain buffer.").

Therefore, taking the combined teachings of Furuhashi, Yammamoto and Wang, as a whole, it would have been obvious to a person having ordinary skill in the art to incorporate the output buffer taught by Wang to the source driver of Furuhashi and

Yammamoto to obtain a source driver with a buffer connected to DAC to perform the data line driving for every state of the driver (Col. 1, lines 23 – 32).

Re claim 9, the combined teachings of Furuhashi, Yammamoto and Wang as a whole teach the source driver of claim 8, wherein the digital-to-analog converter with the negative polarity provides an image data conversion with the negative polarity (Col. 6, lines 8 – 12; "the digital-to-analog converting circuit can be constructed as to produce the lcd apply voltages having the positive polarity and the negative polarity.").

The limitations of claim 10 are substantially similar to the limitations of claim 8. Therefore it has been analyzed and rejected similar to the rejection of claim 8.

Allowable Subject Matter

7. Claims 2 and 3 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

8. Claims 11 - 24 are allowed.

9. The following is an examiner's statement of reasons for allowance:

Furuhashi et al. (US 5,731,796) teach a method for driving a liquid crystal display apparatus that includes an LCD panel arranged by a plurality of pixel units formed in a matrix shape, and a signal drive circuit for generating an LCD apply voltage and constructed of at least two integrated circuits.

Wang et al. (US 6,552,708) teach a unit gain buffer of a driver circuit to drive the data line in the filed of LCD data driver.

Yamamoto et al. (US 6,552,708 B1) teach the amplitude expansion circuit as a main part of a drive circuit which includes a VM DC power supply line to which a voltage VM is applied; a VH DC power supply to which a voltage VH roughly twice as high as the voltage VM is applied.

None of the prior art teaches an analog circuit with positive polarity coupled to a power supply voltage level and a first middle voltage level, and an analog circuit with negative polarity coupled to a ground level and a second middle voltage level.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yong Sim whose telephone number is (571) 270-1189. The examiner can normally be reached on Monday - Friday (Alternate Fridays off) 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

2/01/2007

AMR A. AWAD
SUPERVISORY PATENT EXAMINER